

## CLAIMS

What is claimed is:

- 1      1. A method of integrated circuit design, said method comprising the steps of:  
2            a) identifying critical paths in an integrated circuit design;  
3            b) weighting edges in identified said critical paths  
4            c) assigning net criticality to each weighted edge responsive to edge  
5            weight; and  
6            d) re-placing and wiring nets according to edge criticality.
- 1      2. A method as in claim 1, further comprising before the step (a) of identifying  
2            critical paths, the step of:  
3            a1) placing and wiring said integrated circuit design.
- 1      3. A method as in claim 2 wherein the step (a) of identifying critical paths  
2            further comprises removing non-critical paths from consideration.
- 1      4. A method as in claim 3 wherein step (b) of identifying critical paths  
2            comprises forming a slack graph indicating path slack and edges within said critical  
3            paths, non-critical paths being deleted from said slack graph.
- 1      5. A method as in claim 4 wherein step (c) of weighting edges comprises the  
2            steps of:  
3            i) traversing said critical paths from front to back, an input path weight  
4            being assigned to each edge encountered in said traversal;  
5            ii) traversing each critical path from back to front, an output path weight  
6            being assigned to each encountered edge in said reverse traversal; and  
7            iii) summing said assigned input path weight and said assigned output  
8            path weight for each edge.
- 1      6. A method as in claim 5 wherein assigning net criticality value comprises:  
2            sorting nets according to edge weight;

3                   grouping sorted nets; and  
4                   assigning a criticality value to each group.

1                 7. A method as in claim 6 wherein the step (c) of re-placing and wiring nets  
2                   comprises:

- 3                   i)       selecting an edge having a highest criticality value;  
4                   ii)      adjusting cell placement and net wiring for said selected edge; and  
5                   iii)     checking for remaining critical edges and repeating steps i-ii until no  
6                   critical edges are found.

1                 8. A method as in claim 7 further including prior to the step (iii) of checking for  
2                   remaining critical edges the step of:

- 3                   iiiA)    checking to determine if exit criteria are met and ending if said exit  
4                   criteria are met.

1                 9. A computer-readable medium having stored thereon a plurality of  
2                   instructions, the plurality of instructions including instructions which, when  
3                   executed by a processor, cause the processor to:

- 4                   a)       identify critical paths in an integrated circuit design;  
5                   b)       weight edges in identified said critical path;  
6                   c)       assign net criticality to each weighted edge responsive to edge  
7                   weight; and  
8                   d)       re-place and wire nets according to edge criticality.

1                 10. A computer readable medium as in claim 9, identifying critical paths of step  
2                   (a) causing the processor to:

- 3                   a1)      place and wire said integrated circuit design.

1                 11. A computer readable medium as in claim 10 wherein the step (a) of  
2                   identifying critical paths removes non-critical paths from consideration.

1       12. A computer readable medium as in claim 11 wherein identifying critical  
2       paths comprises forming a slack graph indicating path slack and edges within said  
3       critical paths, non-critical paths being deleted from said slack graph.

1       13. A computer medium as in claim 12 wherein step (c) of weighting edges  
2       causes the processor to:

- 3           i)      traverse said critical paths from front to back and assign an input path  
4       weight to each edge encountered in said traversal;
- 5           ii)     traverse each critical path from back to front and assign an output  
6       path weight to each encountered edge in said reverse traversal; and
- 7           iii)    sum said assigned input path weight and said assigned output path  
8       weight for each edge.

1       14. A computer readable medium as in claim 13 wherein assigning criticality  
2       causes the processor to:

- 3       sort nets according to edge weight;
- 4       group sorted nets; and
- 5       assign a criticality value to each group.

1       15. A computer readable medium as in claim 14 wherein re-placing and wiring  
2       nets causes the processor to:

- 3           i)      select an edge having a highest criticality value;
- 4           ii)     adjust cell placement and net wiring for said selected edge; and
- 5           iii)    check for remaining critical edges and repeat i-ii until no critical  
6       edges are found.

1       16. A computer medium as in claim 15 wherein if exit criteria are met, said  
2       processor is caused to end prior to selecting and adjusting all critical edges.